5 V, 3 A Logic Controlled High-Side or Low-Side Load Switch

Data Sheet **ADP1196**

FEATURES

- Low RDS_{ON} of 10 mΩ in 6-ball WLCSP
- Wide input voltage range: 0 V to 5.5 V
- 3 A continuous operating current at 70°C
- Bias supply voltage range: 1.83 V to 5.5 V
- Low 26 µA ground (quiescent) current, $V_{IN} \leq 3.4$ V
- Low 50 µA quiescent current, $V_{IN} = 5.5$ V
- Overtemperature protection circuitry
- Low shutdown current: <3.5 µA
- Ultrasmall 1.0 mm × 1.5 mm, 6-ball, 0.5 mm pitch WLCSP

APPLICATIONS

- Communications and infrastructure
  - Thermoelectric cooler (TEC) controller reverse polarity for heating and cooling
  - Fine line geometry core voltage inrush current control
- Medical and healthcare
- Instrumentation

TYPICAL APPLICATIONS CIRCUITS

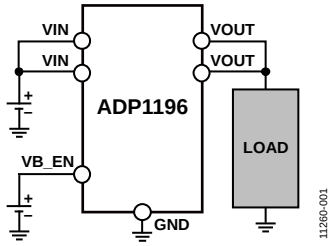

Figure 1. Low-Side Load Application

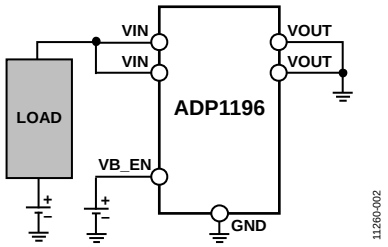

Figure 2. High-Side Load Application

GENERAL DESCRIPTION

The ADP1196 is a high-side or low-side load switch designed for VIN operation between 0 V and 5.5 V with a VB_EN supply of 1.83 V to 5.5 V. The device contains an internal charge pump that operates from either VIN or VB_EN, whichever is higher, and an ultralow on resistance, N-channel MOSFET. This N-channel MOSFET supports more than 2 A of continuous current at VIN close to 0 V, and, with its ultralow on resistance, minimizes power loss. In addition, the on resistance is constant, independent of the VIN or VB_EN voltage. The low 26 µA quiescent current and ultralow shutdown current make the ADP1196 ideal for low power applications.

When the junction temperature exceeds 125°C, overtemperature protection circuitry is activated, thereby protecting the ADP1196 and downstream circuits from potential damage.

The ADP1196 occupies minimal printed circuit board (PCB) space, with an area of less than 1.5 mm^2 and a height of 0.60 mm.

The ADP1196 is available in an ultrasmall 1.0 mm × 1.5 mm, 6-ball, 0.5 mm pitch WLCSP.

Rev. 0 Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2013 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features 1
Applications 1
Typical Applications Circuits 1
General Description 1
Revision History 2
Specifications 3
Timing Diagram 3
Absolute Maximum Ratings 4
Thermal Resistance 4
ESD Caution 4
Pin Configuration and Function Descriptions 5
Typical Performance Characteristics 6
Theory of Operation 9
Applications Information 10
Capacitor Selection 10
Ground Current 10
Enable Feature 10
Timing 11
Current-Limit and Thermal Overload Protection 11
Outline Dimensions 12
Ordering Guide 12

REVISION HISTORY

6/13—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 1.8 V, V_{VB_EN} = 1.83 V, I_{OUT} = 1 A, T_A = 25°C, T_J = −40°C to +85°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		0		5.5	V
BIAS SUPPLY VOLTAGE RANGE	V_{VB_EN}		1.83		5.5	V
ENABLE						
VB_EN Input	V_{IH}	V_{IN} < 1.8 V			1.83	V
	V_{IL}	V_{IN} < 1.8 V	1.6			V
	V_{IH}	V_{IN} = 1.8 V to 5.5 V	1.2			V
	V_{IL}	V_{IN} = 1.8 V to 5.5 V			0.4	V
VB_EN Pull-Down Resistor	I_{EN}	V_{VB_EN} = 400 mV		4		MΩ
CURRENT						
Ground (Quiescent) Current	I_{GND}	V_{IN} = 1.83 V, 1.2 V < V_{VB_EN} < 1.8 V or V_{VB_EN} = 1.83 V, V_{IN} = 0.1 V		26	50	µA
		V_{IN} = 3.4 V, 1.2 V < V_{VB_EN} < 1.8 V or V_{VB_EN} = 3.4 V, V_{IN} = 0.1 V		26		µA
		V_{IN} = 4.2 V, 1.2 V < V_{VB_EN} < 1.8 V or V_{VB_EN} = 4.2 V, V_{IN} = 0.1 V		35	50	µA
		V_{IN} = 5.5 V, 1.2 V < V_{VB_EN} < 1.8 V or V_{VB_EN} = 5.5 V, V_{IN} = 0.1 V		50	68	µA
Shutdown Current	I_{OFF}	V_{VB_EN} = GND, V_{OUT} = 0 V, V_{IN} = 4.2 V		3.5		µA
		V_{VB_EN} = GND, V_{OUT} = 0 V, V_{IN} = 1.8 V to 5.5 V			40	µA
Continuous Operating Current[1]	I_{OUT}	V_{IN} = 1.83 V to 5.5 V, V_{VB_EN} > 1.2 V or V_{VB_EN} = 1.83 V to 5.5 V, V_{IN} = 0.1 V to V_{VB_EN}		3		A
VIN TO VOUT RESISTANCE	RDS_{ON}					
		V_{IN} = 5.5 V, V_{VB_EN} > 1.2 V or V_{VB_EN} = 5.5 V, V_{IN} = 0.1 V		0.01	0.015	Ω
		V_{IN} = 4.2 V, V_{VB_EN} > 1.2 V or V_{VB_EN} = 4.2 V, V_{IN} = 0.1 V		0.01	0.015	Ω
		V_{IN} = 1.83 V, V_{VB_EN} > 1.2 V or V_{VB_EN} = 1.83 V, V_{IN} = 0.1 V		0.01	0.015	Ω
V_{OUT} TURN-ON DELAY TIME		See Figure 3				
Turn-On Delay Time	t_{ON_DLY}	V_{IN} = 1.83 V to 5.5 V, V_{VB_EN} > 1.2 V, C_{LOAD} = 1 µF		2		ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		125		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C

[1] At an ambient temperature of 85°C, the part can withstand a continuous current of ±2.22 A. At a load current of 3 A, the operational lifetime derates to 2190 hours.

TIMING DIAGRAM

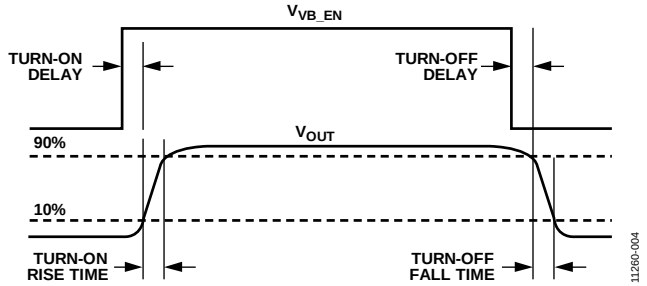

Figure 3. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
VOUT to GND	−0.3 V to VIN
VB_EN to GND	−0.3 V to +6.5 V
Continuous Drain Current	
T_A = 25°C	±4 A
T_A = 85°C	±2.22 A
Continuous Diode Current	−50 mA
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +105°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Typical θ_{JA} and Ψ_{JB} Values

Package Type	θ_{JA}	Ψ_{JB}	Unit
6-Ball, 0.5 mm Pitch WLCSP	260	58	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

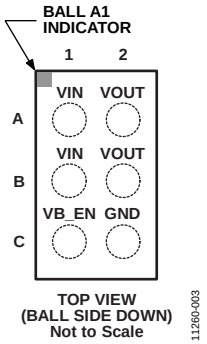

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, B1	VIN	Input Voltage.
A2, B2	VOUT	Output Voltage.
C1	VB_EN	Enable/Bias Input. Drive VB_EN high to turn on the switch, and drive VB_EN low to turn off the switch.
C2	GND	Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 1.8 V, V_{VB_EN} = 1.83 V, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

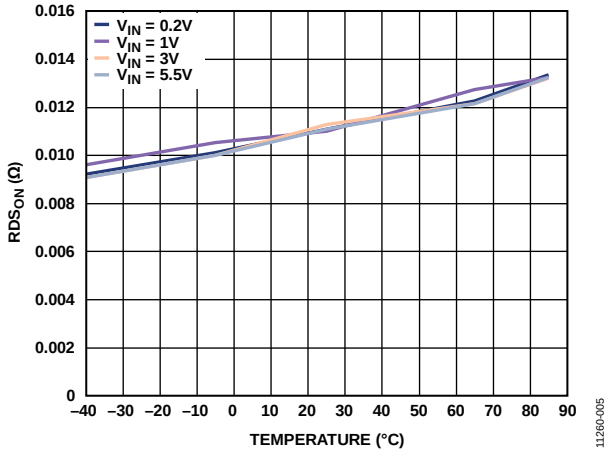

Figure 5. RDS_{ON} vs. Temperature, 50 mA, Different Input Voltages (V_{IN})

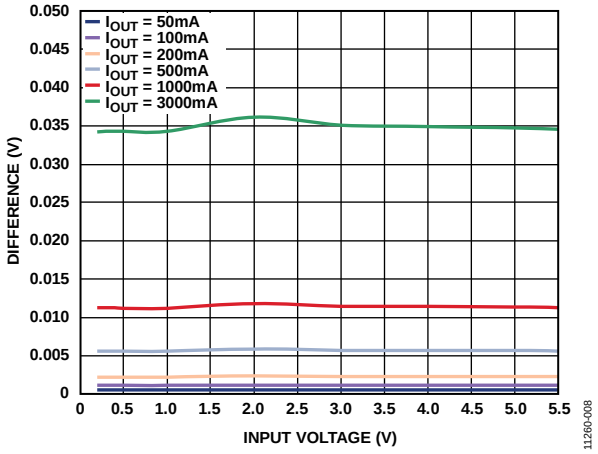

Figure 8. Voltage Drop vs. Input Voltage (V_{IN}), Different Load Currents

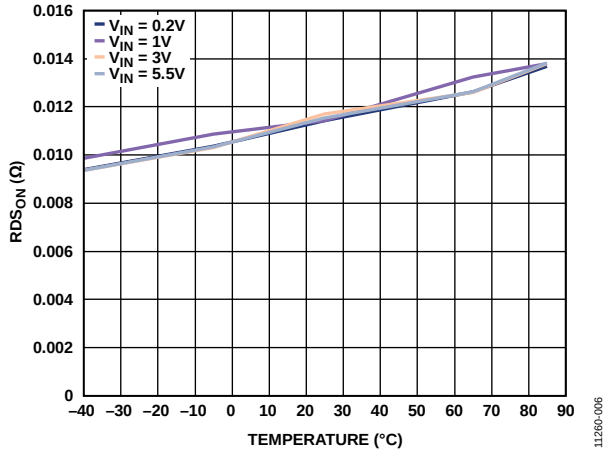

Figure 6. RDS_{ON} vs. Temperature, 3 A, Different Input Voltages (V_{IN})

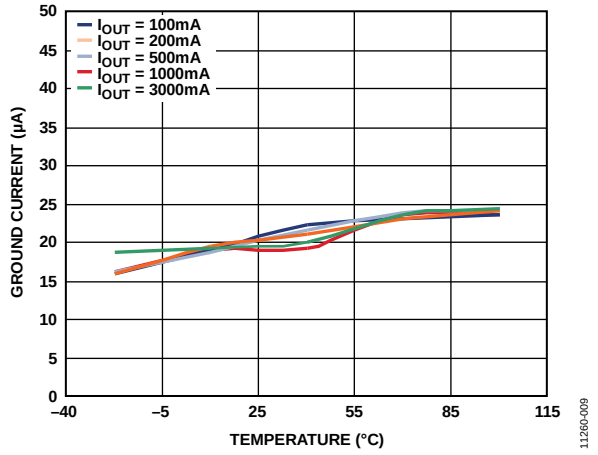

Figure 9. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 1.8 V

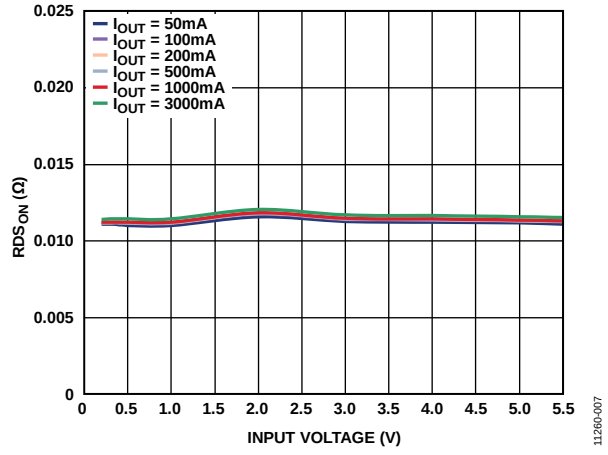

Figure 7. RDS_{ON} vs. Input Voltage (V_{IN}), Different Load Currents

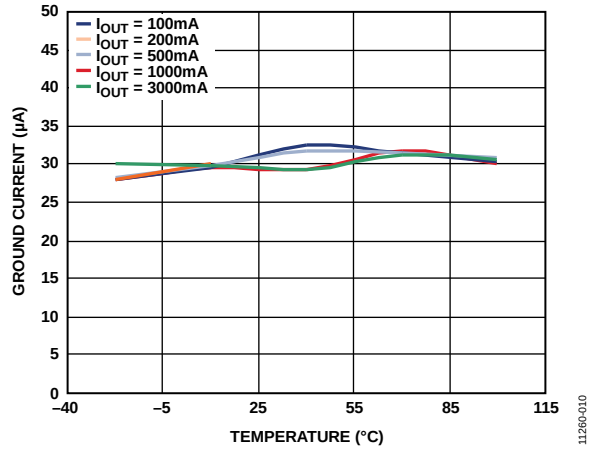

Figure 10. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 3.6 V

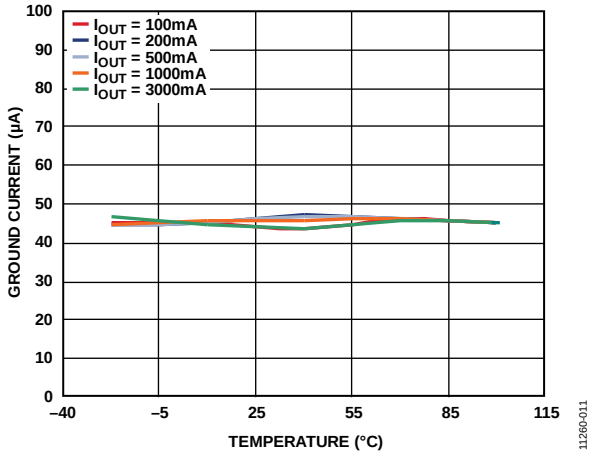

Figure 11. Ground Current vs. Temperature, Different Load Currents, V_{IN} = 5 V

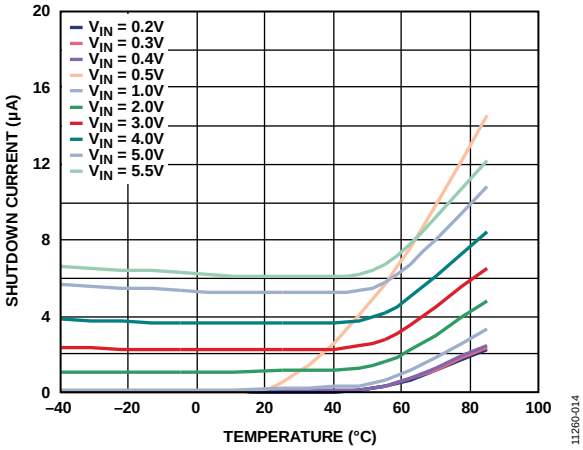

Figure 14. Shutdown Current vs. Temperature, V_{OUT} = 0 V, Different Input Voltages (V_{IN})

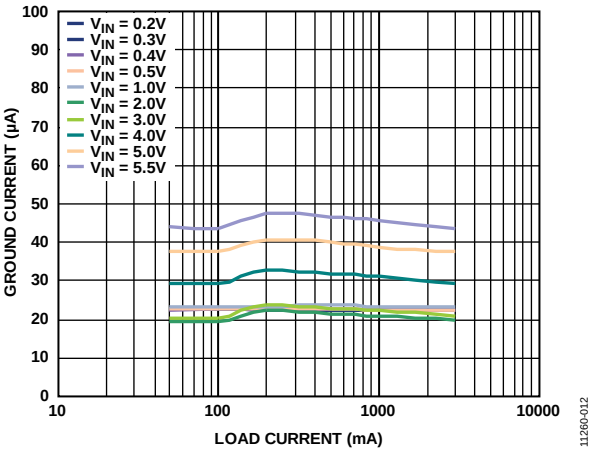

Figure 12. Ground Current vs. Load Current, Different Input Voltages (V_{IN})

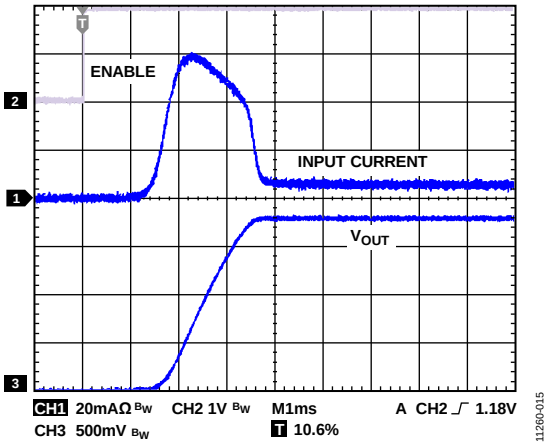

Figure 15. Typical Turn-On Time and Inrush Current, V_{IN} = 1.8 V, C_{OUT} = 47 µF, 330 Ω Load

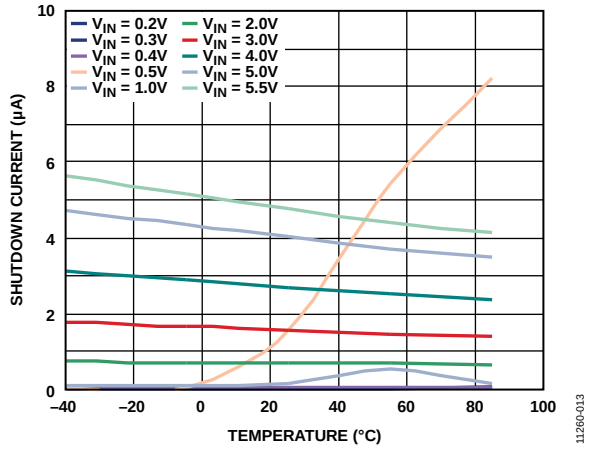

Figure 13. Shutdown Current vs. Temperature, Different Input Voltages (V_{IN}), V_{OUT} Open

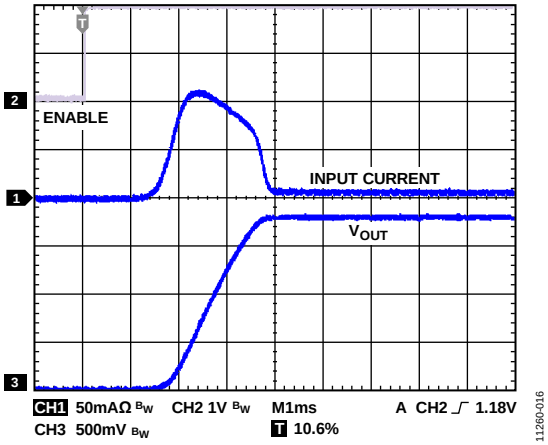

Figure 16. Typical Turn-On Time and Inrush Current, V_{IN} = 1.8 V, C_{OUT} = 100 µF, 330 Ω Load

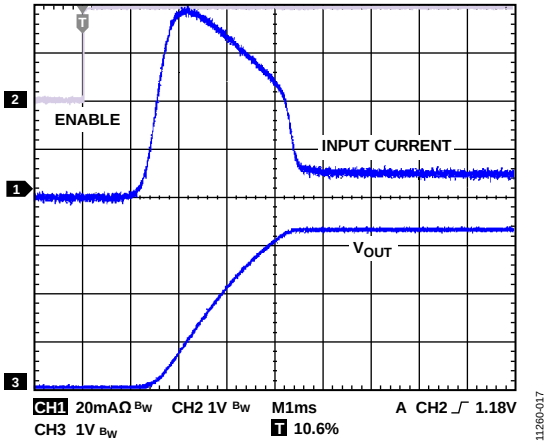

Figure 17. Typical Turn-On Time and Inrush Current, V_{IN} = 3.3 V, C_{OUT} = 47 µF, 330 Ω Load

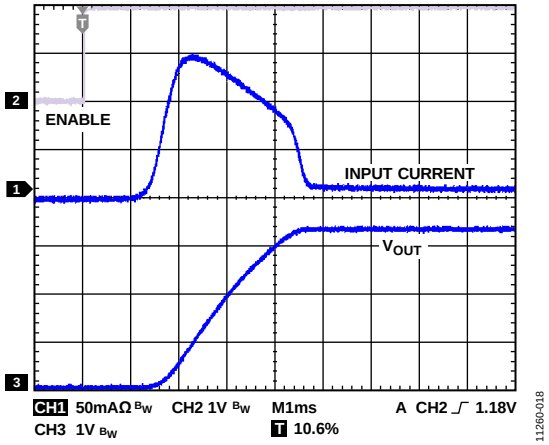

Figure 18. Typical Turn-On Time and Inrush Current, V_{IN} = 3.3 V, C_{OUT} = 100 µF, 330 Ω Load

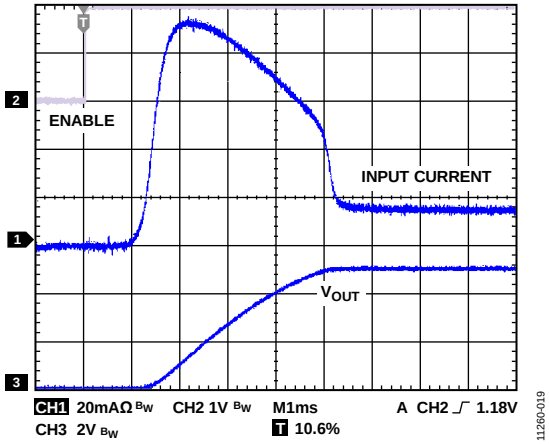

Figure 19. Typical Turn-On Time and Inrush Current, V_{IN} = 5 V, C_{OUT} = 47 µF, 330 Ω Load

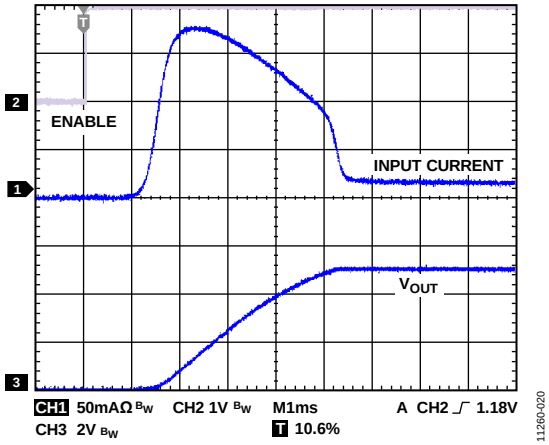

Figure 20. Typical Turn-On Time and Inrush Current, V_{IN} = 5 V, C_{OUT} = 100 µF, 330 Ω Load

THEORY OF OPERATION

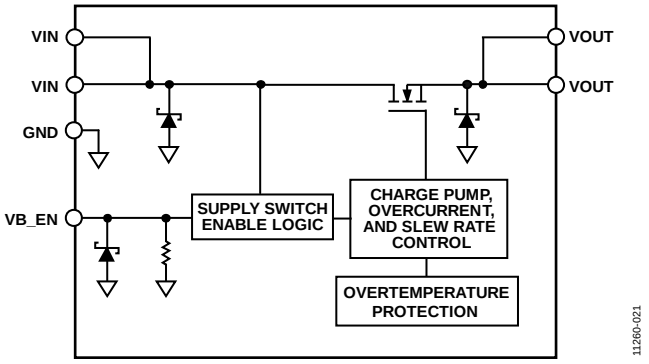

Figure 21. Functional Block Diagram

The ADP1196 is a high-side or low-side N-channel metal oxide semiconductor (NMOS) load switch that is controlled by an internal charge pump. The ADP1196 operates with voltages from 1.83 V to 5.5 V on either VIN or VB_EN.

Internal circuitry monitors the VIN and VB_EN pins, connecting the internal power supply to the higher of the two voltages. This operation allows the NMOS load switch to operate on the low side of a particular load.

An internal charge pump biases the NMOS switch to achieve a relatively constant, ultralow on resistance of 10 mΩ across the entire supply range. The use of the internal charge pump also allows for controlled turn-on times. Turning the NMOS switch on and off is controlled by the enable input, VB_EN, which can interface directly with 1.83 V logic signals when VIN is greater than 1.8 V.

The ADP1196 supports 3 A of continuous current as long as T_A is less than or equal to 70°C. At 85°C, the derated load current falls to ±2.22 A. Overcurrent protection limits the output current to 4 A.

The overtemperature protection circuit is activated if the load current causes the junction temperature to exceed 125°C. When this occurs, the overtemperature protection circuitry disables the output until the junction temperature falls below approximately 110°C, at which point the output is reenabled. If the fault condition persists, the output cycles off and on until the fault is removed.

ESD protection structures are shown in the block diagram as Zener diodes (see Figure 21).

The ADP1196 is a low quiescent current device with a nominal 4 MΩ pull-down resistor on its enable pin (VB_EN). The package is a space-saving 1.0 mm × 1.5 mm, 6-ball WLCSP.

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1196 is designed for operation with small, space-saving ceramic capacitors; however, it functions with most commonly used capacitors when the effective series resistance (ESR) value is carefully considered. The ESR of the output capacitor affects the response to load transients. Use a typical 1 µF capacitor with an ESR of 0.1 Ω or less for good transient response. Using a larger value of output capacitance improves the transient response to large changes in load current.

Input Bypass Capacitor

Connecting at least 1 µF of capacitance from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when high source impedance or long input traces are encountered. When greater than 1 µF of output capacitance is required, increase the input capacitor to match it.

GROUND CURRENT

The major source of ground current in the ADP1196 is the internal charge pump for the field effect transistor (FET) drive circuitry. Figure 22 shows the typical ground current when V_{VB_EN} = 1.83 V and V_{IN} varies from 0.2 V to 5.5 V.

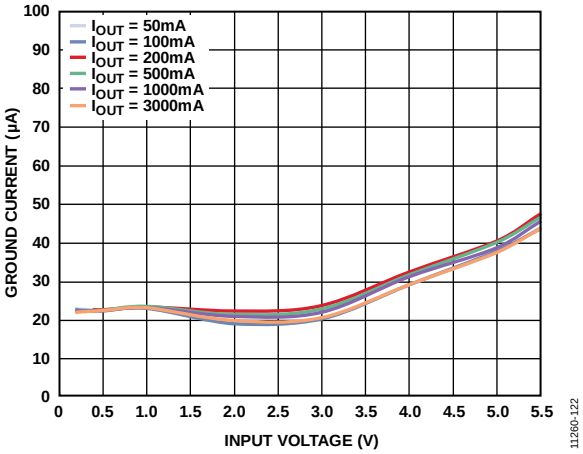

Figure 22. Ground Current vs. Input Voltage, Different Load Currents

ENABLE FEATURE

The ADP1196 uses the VB_EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 23, when a rising voltage (V_{VB_EN}) on the VB_EN pin crosses the active threshold, VOUT turns on. When a falling voltage (V_{VB_EN}) on the VB_EN pin crosses the inactive threshold, VOUT turns off.

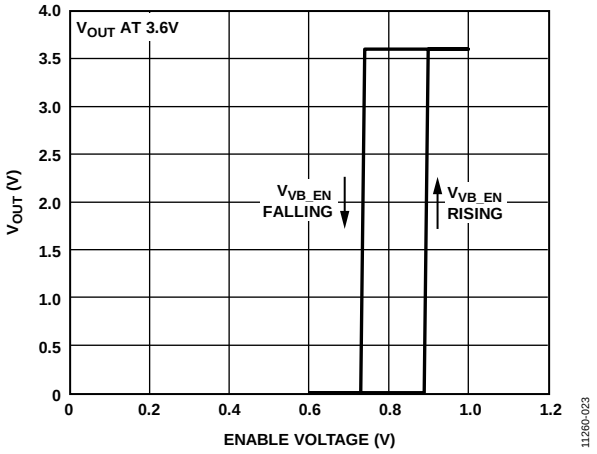

Figure 23. Typical VB_EN Operation

As shown in Figure 23, the VB_EN pin has hysteresis built into it. This built-in hysteresis prevents on/off oscillations that can occur due to noise on the VB_EN pin as it passes through the threshold points.

The VB_EN pin active/inactive thresholds derive from the V_{IN} voltage; therefore, these thresholds vary with changing input voltages. Figure 24 shows the typical VB_EN active/inactive threshold when the input voltage varies from 1.83 V to 5.5 V.

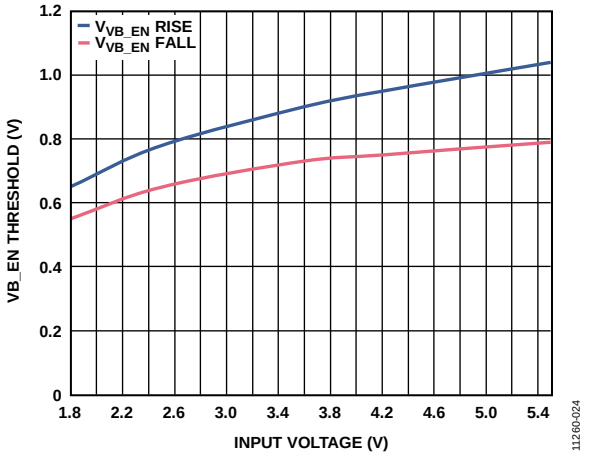

Figure 24. Typical VB_EN Threshold vs. Input Voltage (V_{IN})

TIMING

Turn-on delay is defined as the interval between the time that V_{VB_EN} exceeds the rising threshold voltage and when V_{OUT} rises to ~10% of its final value. The ADP1196 includes circuitry that has a typical 2 ms turn-on delay and a controlled rise time to limit the V_{IN} inrush current. As shown in Figure 25 and Figure 26, the turn-on delay is nearly independent of the input voltage.

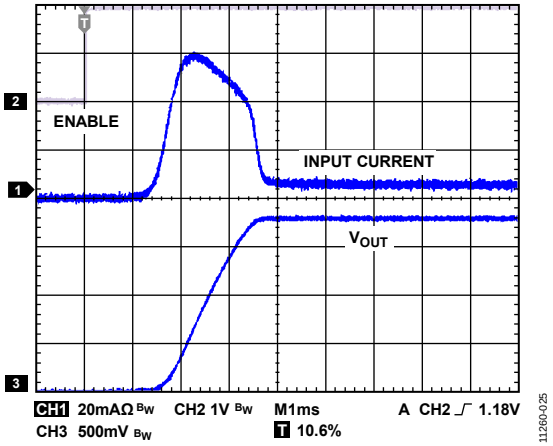

Figure 25. Typical Turn-On Time and Inrush Current, V_{IN} = 1.8 V, C_{OUT} = 47 µF, 330 Ω Load

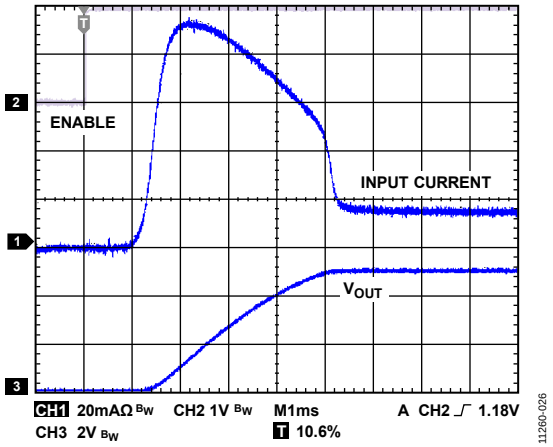

Figure 26. Typical Turn-On Time and Inrush Current, V_{IN} = 5 V, C_{OUT} = 47 µF, 330 Ω Load

The rise time is defined as the time it takes the output voltage (V_{OUT}) to rise from 10% to 90% of its final value. The output voltage rise time is dependent on the rise time of the internal charge pump.

For very large values of output capacitance, the RC time constant (where C is the load capacitance (C_{LOAD}) and R is the $RDS_{ON}||R_{LOAD}$) can become a factor in the rise time of the output voltage. Because RDS_{ON} is much smaller than R_{LOAD}, an adequate approximation for RC is $RDS_{ON} \times C_{LOAD}$. An input or load capacitor is not required for the ADP1196, although capacitors can be used to suppress noise on the board.

The turn-off time is defined as the time it takes for the output voltage to fall from 90% to 10% of V_{OUT}. It is also dependent on the RC time constant of the output capacitance and load resistance. Figure 27 shows the typical turn-off times with V_{IN} = 1.8 V, V_{IN} = 3.3 V, and V_{IN} = 5.0 V, C_{OUT} = 47 µF, and R_{LOAD} = 330 Ω.

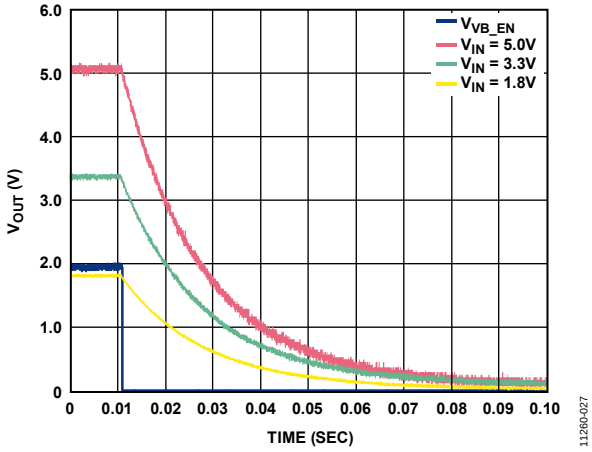

Figure 27. Typical Turn-Off Time, V_{IN} = 1.8 , V_{IN} = 3.3 V, and V_{IN} = 5.0 V, C_{OUT} = 47 µF, R_{LOAD} = 330 Ω

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1196 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP1196 is designed to limit current when the output load reaches 4 A. When the output load exceeds 4 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 125°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation), when the junction temperature starts to rise above 125°C, the output is turned off, reducing the output current to zero. When the junction temperature falls below 110°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP1196 limits current, so that only 4 A conducts into the short. If the self-heating of the junction is great enough to cause its temperature to rise above 125°C, thermal shutdown is activated, turning off the output and reducing the output current to zero. As the junction temperature cools and falls below 110°C, the output turns on and conducts 4 A into the short, again causing the junction temperature to rise above 125°C. This thermal oscillation between 110°C and 125°C causes a current oscillation between 4 A and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperature does not exceed 125°C.

OUTLINE DIMENSIONS

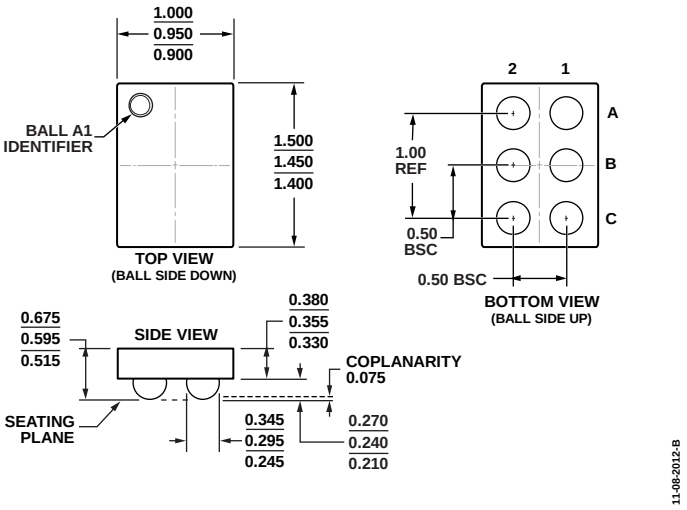

Figure 28. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADP1196ACBZ-R7	−40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	BW

[1] Z = RoHS Compliant Part.

©2013 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D11260-0-6/13(0)